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ATTENTION:	*Examiner:* PAN, DANIEL H. *Art Unit:* 2183	

From:		Telephone No.:
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Re:	*Serial No.:* 09/801,080	
	Attorney Docket No.: NL000133	

TRANSMISSION INCLUDES: 13 Pages (including cover sheet)

Transmittal of Brief in Support of Appeal - 1 page

Appeal Brief - 11 pages

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on 8/8/06 by Vilimaina Naga

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IN THE UNTED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

First-Named Inventor:BUSA, Natalino Giorgio	Atty Docket No.: **NL000133**
Application No.:09/801,080 Conf.: 5082	Art Unit: 2183
Date Filed: 03/07/2001	Examiner: PAN, DANIEL H
Customer No.: 24738	

Title: Data Processing Device, Method of Operating a Data Processing Device and Method for Compiling a Program

Mail Stop Appeal Brief-Patents
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TRANSMITTAL OF
BRIEF IN SUPPORT OF AN APPEAL

Sir:

Enclosed is an Appeal Brief in the above-identified patent application.

Please charge the any and all required fees to Deposit Account No. 14-1270.

Date: AUG-8-2006

Respectfully submitted,
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(Date) 8/8/06 (Signature) _____
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application

Inventor	:	**Busa**
Application No.	:	**09/801,080**
Filed	:	**03/07/2001**
For	:	**Data processing device, method of operating a data processing device and method for compiling a program**

APPEAL BRIEF

On Appeal from Group Art Unit 2183

Date: July 27, 2006

By: Michael Ure
Attorney for Applicant
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Vilimaina Naga
(Name)

8/8/06
(Signature and Date)

TABLE OF CONTENTS

		Page
I.	REAL PARTY IN INTEREST.....	3
II.	RELATED APPEALS AND INTERFERENCES.....	3
III.	STATUS OF CLAIMS.....	3
IV.	STATUS OF AMENDMENTS.....	3
V.	SUMMARY OF THE CLAIMED SUBJECT MATTER ..	3
VI.	GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL	4
VII.	ARGUMENT.....	5
VIII.	CONCLUSION.....	7
	APPENDICES: THE CLAIMS ON APPEAL.....	8
	RELATED PROCEEDINGS	
	EVIDENCE	

TABLE OF CASES

NONE

I. REAL PARTY IN INTEREST

The real party in interest is the assignee of the present application, Koninklijke Philips Electronics N.V., and not the party named in the above caption.

II. RELATED APPEALS AND INTERFERENCES

With regard to identifying by number and filing date all other appeals or interferences known to Appellant which will directly effect or be directly affected by or have a bearing on the Board's decision in this appeal, Appellant is not aware of any such appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-5 are pending, stand finally rejected, and forms the subject matter of the present appeal.

IV. STATUS OF AMENDMENTS

All amendments have been entered. No amendment after final rejection has been submitted.

V. SUMMARY of the CLAIMED SUBJECT MATTER

The present invention relates, in one aspect, to a computational method in which one functional unit, during execution of an instruction, outputs data to or receives input data from another functional unit *during execution of the instruction*, where the functional units share a common memory, e.g., a micro code memory. Claims 1, 4 and 6 have been amended to make clear that such input/output occurs during execution of the

instruction. Figures 6a and 6b illustrate a particular computation (that of Figure 5, which in turn references the 2Dtransform operation of Figure 2) performed conventionally (Figure 6a) and using the computational method of the present invention (Figure 6b). In the illustrated example, the computational method of the invention results in a 20% reduction in computation time.

The foregoing example is described more particularly in the present specification at page 10, line 27, to page 6, line 19. In Figure 6a, the 2Dtransform operation (Figure 2) is performed *atomically*; i.e., inputs are presented simultaneously to a complex functional unit, which performs the operation and presents outputs simultaneously. In Figure 6b, by contrast, inputs are not presented simultaneously, nor are outputs presented simultaneously. The input i_1 (= p + q) is presented to the complex functional unit as soon as it is available, in cycle 1. During cycles 1 and 2, the second input i_2 (= p – q – 2) is prepared and is then presented to the complex functional unit in cycle 3. Also in cycle 3, the first output o_1 (= $2*i_2 + 3$) is presented. During cycles 3, 4 and 5, the output o_2 (= $5*i_1 + 2*i_2 + 1$) is computed and presented. During cycles 4 and 5, o_1 (previously made available in cycle 3) is squared and the value 100 is subtracted to form a partial result as part of the condition checking in the last statement of Figure 5. In cycles 6 and 7, o_1 is squared and the resulting quantity added to the partial result. Finally, in cycle 8, the inequality is evaluated. In this example, it may be seen that output data (e.g., o_1) of the complex functional unit ("first functional unit") is processed by the other functional unit ("second functional unit") during execution of the instruction (e.g., 2Dtransform) by the complex functional unit ("first functional unit") as recited in claim 1. Also, input data (e.g., i_2) to the first functional unit is generated by the second functional unit during execution of the instruction as recited in claim 1.

VI. GROUNDS of REJECTION to be REVIEWED ON APPEAL

The issues in the present matter are whether:

1. claims 1-5 are anticipated by O'Connor.
2. claims 1-5 are anticipated by McNeill.

VII. ARGUMENT

I. Rejection of Claims 1-5 as anticipated by O'Connor

The O'Connor reference teaches something quite different. O'Connor relates to "scoreboarding," a method of resource arbitration in which a centralized set of tables ("registers") in the CPU keep track of what is being used and when. Each row indicates what is being used at each clock tick. Scoreboarding is used to manage dispatch, stalling, and completion of instructions, to watches for Write-After-Write, Read-After-Write and Write-After-Read (WAW, RAW, WAR) hazards, and to manage the execution sequence (e.g. possible instruction reordering) to avoid these hazards. Hazards are detected by observing register references and operation types.

In particular, O'Connor describes a hardware-efficient implementation of a bypass circuit that that enables a result from one execution unit to be provided to a waiting execution unit at the same time that result is sent to a register.

In O'Connor, one execution unit waits for results from another execution unit in order for the first execution unit to begin execution. The execution units do not operate concurrently to achieve execution of an instruction.

II. Rejection of Claims 1-5 as anticipated by McNeill

The rejection based on McNeill ignores the basic distinction between an *instruction* and a computing *task*. An instruction is a well-defined operation that takes a known number of clock cycles of a functional unit. A computing task, on the other hand, is performed by executing a series of instructions in sequence. The time required to perform the computing task is often indeterminate.

In McNeill, a slave CPU performs a search on data supplied through a disk interface. Such a search is a computing task. It is not "an instruction" as set forth in the present claims.

In view of the above, applicant submits that all of the above referred-to claims are patentable over the teachings of the cited references.

VIII. CONCLUSION

In view of the above analysis, it is respectfully submitted that the referenced teachings, whether taken individually or in combination, fail to anticipate or render obvious the subject matter of any of the present claims. Therefore, reversal of all outstanding grounds of rejection is respectfully solicited.

Date: ~~07/27/2006~~ 8/8/2006

By: Michael Ure
Attorney for Applicant
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IX. APPENDIX: THE CLAIMS ON APPEAL

1. A data processing device, comprising a master controller, a first functional unit including a slave controller, a second functional unit, and a common memory means shared by the first and second functional units, the data processing device being programmed for executing an instruction by the first functional unit, execution of said instruction involving input/output operations by the first functional unit, wherein said execution involves at least one of: output data of the first functional unit being processed by the second functional unit during execution of said instruction, and the input data to the first functional unit being generated by the second functional unit during execution of said instruction.

2. The data processing device according to claim 1, wherein the first functional unit is arranged for processing instructions of a first type corresponding to operations having a relatively large latency and the second functional unit is arranged for processing instructions of a second type corresponding to operations having a relatively small latency.

3. The data processing device according to claim 1, having halt means controllable by the master controller for suspending operation of the first functional unit.

4. A method of operating a data processing device, comprising:

a master controller for controlling operation of the data processing device,

a first functional unit, which includes a slave controller, the first functional unit being arranged for executing instructions of a first type corresponding to operations having a relatively long latency,

a second functional unit capable of executing instructions of a second type corresponding to operations having a relatively short latency, wherein the first functional unit during execution of an instruction of the first type receives input data and provides output data, and said execution involves at least one of: output data of the first functional unit being processed by the second functional unit during execution of said instruction, and input data to the first functional unit being generated by the second functional unit during execution of said instruction.

5. The method according to claim 4, wherein the master controller temporarily suspends operation of the first functional unit during execution of instructions of the first type.

X. APPENDIX: RELATED PROCEEDINGS

NONE

XI. APPENDIX: EVIDENCE

NONE